

10/054,964

Serial No. 10/054,964

Docket No. KY-172

Response to Ex Parte Quayle Action dated January 24, 2007

Response to Ex Parte Quayle Action mailed November 24, 2006

frequency of the ring oscillator 12 is PLL-controlled such that it coincident with a frequency of the external clock signal CLK.

5.6.  
3.5.07  
On page <sup>17</sup>18, at line <sup>29</sup>7, please amend the paragraph as follows:

The synthesizing ratio 1:4 is selected under assumption that the voltage for regulating the characteristics of the inverters 13a of the delay line 13 is about 20% of the voltage  $V_S - V_s$  of the power source line 14 of the ring oscillator 12 as a reference.